Tuesday, August 30

DSD Tutorial Day (for details see http://dsd2005.univ-rennes1.fr/)

Wednesday, August 31

8:30-9:30	60 min	**Registration**
9:30-10:00	30 min	***Opening Session***
10:00-11:00	60 min	Keynote Speech **Software Process Improvement in agile environments - industry perspectives and research methods** *Pekka Abrahamsson*
11:00-11:30	30 min	Coffee break
12:00-13:00	60 min	Keynote Speech *Chair.A.Nunez* **Multi-media applications and imprecise computation** *Melvin A. Breuer*
12:30-14:00	90 min	Lunch

Wednesday, August 31

14:00-15:00

SS2: Dependability and Testing of Digital Systems (S1)
Part 1. ***Chair H. Kubatova***

14:00-15:00	30 min	(29) BIST TECHNIQUE FOR GALS SYSTEMS *Milos Krstic, Eckhard Grass*
	30 min	(16) Functional Vectors Generation for RT-Level Verilog Descriptions Based on Path Enumeration and Constraint Logic Programming *Tun Li, Dan Zhu, Yang Guo, SiKun Li*

System Synthesis (S2)
Part 1. Power and Component Driven System Synthesis. ***Chair L. Fanucci***

14:00-15:00	30 min	(87) AN INNOVATIVE MDA METHODOLOGY FOR EMBEDDED REAL-TIME SYSTEM *A. Cuccuru, R. De Simone , T. Saunier, G. Siegel, Y. Sorel*
	30 min	(118) Power-Composition Profile Driven Co-Synthesis with Power Management Selection for Dynamic and Leakage Energy Reduction *Dong Wu, Bashir M Al-Hashimi, Marcus Schmitz, Petru Eles*

Circuits Synthesis (S3)
Part 1. Arithmetic. ***Chair T. Sasao***

14:00-15:00	30 min	(27) A Low-Power FIR Filter Using Combined Residue and Radix-2 Signed-Digit Representation *Andreas Lindahl, Lars Bengtsson*
	30 min	(100) Approximating Trigonometric Functions with the Laws of Sines and Cosines using the Logarithmic Number System *Mark G Arnold*

15:00-15:30	30 min	Coffee break

15:30-17:35

SS2: Dependability and Testing of Digital Systems (S4)
Part 2. ***Chair H. Kubatova***

15:30-17:10	30 min	(75) Improvement of the Fault Coverage of the Pseudo-Random Phase in Column Matching BIST *Petr Fiser, Hana Kubatova*
	30 min	(50) Characterization of wavelet-based image coding systems for algorithmic fault detection *Lucía Costas Perez, Juan J. Rodríguez-Andina*
	30 min	(64) Improved Fault Emulation for Synchronous Sequential Circuits *J. Raik, P. Ellervee, V. Tihhomirov, R. Ubar*
	5 min	(60) Defect-Oriented Test- and Layout-Generation for Standard-Cell ASIC Designs J. Sudbrock, J. Raik, R. Ubar, W. Kuzmicz, W. Pleskacz
	5 min	(65) Power-Constrained Hybrid BIST Test Scheduling in an Abort-on-First-Fail Test Environment *Zhiyuan He, Gert Jervan, Zebo Peng, Petru Eles*

System Synthesis (S5)
Part 2. Component Based System Synthesis. ***Chair K. Waldschmidt***

15:30-17:00	30 min	(104) HARDWARE DESIGN BASED ON VIRTUAL COMPONENT SYNTHESIS *A.Fouilliart, N.Abdelli, E.Casseau, B.Le Gall, Ch.Jego, N.Heno*
	30 min	(105) High-Level Synthesis for DVB-DSNG modem in an Optimized Latency Insensitive System Context *N.Abdelli, P.Bomel, P.Kajfasz, E.Martin, E.Boutillon, A.Fouilliart*
	15 min	(53) Embedded Object architecture *Tero Vallius, Juha Röning*
	15 min	(13) An Effective Framework for Enabling the Reuse of External Soft IP Soujanna Sarkar, Subash Chandar G.

Circuits Synthesis (S6)
Part 2. Logic Synthesis. ***Chair T. Luba***

15:30-17:15	30 min	(97) A novel method of two-stage decomposition dedicated for PAL-based CPLDs) *Dariusz Kania, Józef Kulisz, Adam Milik*
	15 min	(116) An Advanced Minimization Technique for Multiple Valued Multiple Output Logic Expressions Using LUT and Realization Using Current Mode CMOS *Md.S.Shahriar, M.A.R. Mustafa et al.*
	15 min	(93) State assignment for PAL-based CPLDs *Robert Czerwinski, Dariusz Kania*
	5 min	(23) Coefficient Bit Reordering Method for Configurable FIR Filtering on Folded Bit-plane Array *Vladimir Ciric, Ivan Milentijevic*
	5 min	(34) Automatic Design of Binary and Multiple-Valued Logic Gates on the RTD Series *Krzysztof S. Berezowski, Sarma B. K. Vrudhula*

15 min	Poster Session: Papers [60, 65,13, 23, 34]

Thursday, September 1

9:00-10:00	60 min	Keynote Speech **Conmponent-based approach exploit at Philips** *Rob van Ommering*
10:00-11:00	60 min	Keynote Speech *Chair L.Jozwiak* **SoC Design for Advanced Applications** *Bernard CANDAELE*
11:00-11:30	30 min	Coffee break
10:30-12:00	60 min	Keynote Speech *Chair L.Jozwiak* **Wireless Sensor Systems - Constraints and Future Prospect** *Dirk Timmermann*
12:30-14:00	90 min	Lunch

Thursday, September 1

14:00-15:30

SS1: Wireless Sensor Systems (S7)
Part 1. ***Chair Matthias Handy***

14:00-15:20	30 min	(30) Design of Transport Triggered Architecture Processors for Wireless Encryption *P.Hämäläinen,J.Heikkinen,M.Hännikäinen,T.Hämäläinen*
	30 min	Mixed Signal CMOS Circuits for Ad-Hoc Networks (*Invited paper*) *C. Siu, K. Iniewski, F. Nabky, M. El-Gamal, K. Townsend, J. Haslett*
	5 min	(59) Co-simulation of Wireless Local Area Network Terminals with Protocol Software Implemented in SDL *Petri Kukkala, Marko Hännikäinen, Timo D. Hämäläinen*
	5 min	(73) Optimization of Electronic Power Consumption in Wireless Sensor Nodes *Y.Manoli, S.K.Ramachandran, S.K.Jayapal, R.Bhutada, R.Huang*
	5 min	(109) Vital Signs Remote Management System for PDA *Danielly Cruz, Edna Barros*

Verification Techniques (S8)
Part 1. ***Chair S. Ruelke***

14:00-15:15	30 min	(17) MA2TG: A Functional Test Program Generator for Microprocessor Verification *Tun Li, Dan Zhu, Yang Guo, SiKun Li*
	30 min	(76) A processor for testing mixed-signal cores in System-on-Chip *F. Duarte,J. Machado SIlva, J.Carlos Alves, J.Silva*
	5 min	(37) Functional test generation remote tool *(E. Bareisa, V. Jusas, K. Motiejunas, R. Seinauskas)*
	5 min	(115) Validation of Embedded Systems using Formal Method aided Simulation *Daniel Karlsson, Petru Eles, Zebo Peng*

Application Specific Architectures (S9)
Part 1. ***Chair J.Sosnowski***

14:00-15:20	30 min	(35) VLSI Design of a High–Throughput Multi–Rate Decoder for Structured LDPC Codes *M. Rovini, Nicola E. L`Insalata, F. Rossi, Luca Fanucci*
	5 min	(74) A FPGA Based Design of a Multiplierless and Fully Pipelined JPEG Compressor *L.V. Agostini, R.E. Carvalho Porto, I.Saraiva Silva, S.Bampi*
	5 min	(98) Reconfigurable Parallel Approximate String Matching on FPGAs *Jin Hwan Park*
	5 min	(111) Efficient MLP Digital Implementation on FPGA *S. Vitabile, V. Conti, F. Gennaro, F. Sorbello*
	5 min	(47) Designing a Binary Neural Network Co-processor *Michael freeman, Jim austin*
	5 min	(80) Efficient Host-Independent Coprocessor Architecture for Speech Coding Algorithms *H. Safizadeh, H. Noori, M. Sedighi, A. Jahanian, N. Zolfaghari*
	5 min	(57) Massively Parallel Hardware Architecture for Genetic Algorithms *Nadia Nedjah, Luiza de Macedo Mourelle*
	5 min	(122) Implementation of a block based neural branch predictor Oswaldo Cadenas, Graham Megson, Daniel Jones
	5 min	(55) PRUS - PROCESSOR NETWORK FOR DIGITAL CIRCUIT IMPLEMENTATION *S. Hyduke, V. Hahanov, V. Obrizan, O.Guz*
	5 min	(14) Capturing Processor Architectures from Protocol Processing Applications: a Case Study *Seppo Virtanen, Jani Paakkulainen, Tero Nurmi*
	5 min	(83) Yield-aware floorplanning *Zhaojun Wo, Israel Koren, Maciej Ciesielski*

15:30-16;00	30 min	Poster Session: Papers [59, 73, 77, 109, 11, 37, 115, 74, 98, 111, 47, 80, 57, 122, 55, 14, 83]

15:30-16;00	30 min	Coffee break

Thursday, September 1

16:00-18:00

SS1: Wireless Sensor Systems (S10)
Part 2. ***Chair Matthias Handy***

16:00-17:30	30 min	(39) Design of a Development Platform for HW/SW Codesign of Wireless Integrated Sensor Nodes *K. Virk, M.Leopold, A. Vad Lorentzen, M.Hansen, P.Bonnet, J.Madsen*
	30 min	(41) An Efficient MAC Protocol for Sensor Network Considering Energy Consumption and Information Retrieval Pattern *Yashar Ghiassi, Mohammad Mehdi Mansouri*
	30 min	(54) Wireless Sensor Network Implementation for Industrial Linear Position Metering *Mikko Kohvakka, Marko Hännikäinen, Timo D. Hämäläinen*

Verification Techniques (S11)
Part 2. ***Chair***

16:00-17:30	30 min	(52) MemBIST Applet for Learning Principles of Memory Testing and Generating a BIST Structure *(Maria Fischerova, Martin Simlastik)*
	30 min	(62) High-Level Modelling and Detection of the Faulty Behaviour of VOQ Switches under Balanced Traffic *Miguel Pereira-Varela, Enrique Soto-Campos, Juan J. Rodríguez-*
	30 min	(32) Delay testability properties of circuits realizing threshold functions and symmetric functions *Piotr Patronik*

Application Specific Architectures (S12)
Part 2. ***Chair F. Leporati***

16:00-17:30	30 min	(95) A New Architecture for Fast Arithmetic Coding in H.264 Advanced Video Coder *Roberto R. Osorio, Javier D. Bruguera*
	30 min	(114) Exploring Graphics Processor Performance for General Purpose Applications *Pedro Trancoso, Maria Charalambous*
	30 min	(90) Hardware-Based Implementation of the Common Approximate Substring Algorithm Kenneth B. Kent, Sharon Van Schaick, J. E. Rice, P. A. Evan

20:00	**Conference dinner**

Friday, September 2

9:00-10:30

System Synthesis (S13)
Part 3. High Level Language based System Synthesis. ***Chair K. Judmann***

9:00-10:25	30 min	(44) Cost-effective VLSI Design of Non Linear Image Processing Filters *S. Saponara, M. Cassiano, S. Marsi, R. Coen, L. Fanucci*
	30 min	(103) Java to Hardware Compilation for non Data Flow Applications *Per Andersson, Krzysztof Kuchcinski*
	15 min	(8) Formal Communication Semantics of SysetmC {FL} *K.L. Man*
	5 min	(68) A high-level tool for the design of custom image processing systems *Sérgio Martins, José C. Alves*
	5 min	(71) Processing of streams on multiprocessor architecture *Nikolay Kavaldjiev, Gerard J. M. Smit, Pierre G. Jansen*

Reconfigurable Systems (S14)
Part. 1 ***Chair A. Nunez***

9:00-10:25	30 min	(121) A Constraints Programming Approach for Fabric Cell Synthesis *C.Wolinski, K.Kuchcinski*
	30 min	(101) SystemC-based Design Methodology for Reconfigurable System-on-Chip *Yang Qu, Kari Tiensyrjä, Juha-Pekka Soininen*
	15 min	(96) REDUCING INTER-CONFIGURATION MEMORY USAGE AND PERFORMANCE IMPROVEMENT IN RECONFIGURABLE COMPUTING SYSTEMS *Farhad Mehdipour, Morteza Saheb Zamani, Mehdi Sedighi*
	5 min	(113) An adaptive on-line HW/SW Partitioning for soft real time reconfigurable systems *G. Fakhreddine , A. Michel, A. MOHAMED, B.JEMAA Maher*
	5 min	(72) Using a tightly-coupled pipeline in dynamically reconfigurable platform FPGAs Miguel L. Silva, João Canas Ferreira

Data Management in SoC (S15)
Part 1. ***Chair J.S. Matos***

9:00-10:30	30 min	(120) Predictable embedding of large data structures in multiprocessor networks-on-chip Stuijk, Geilen, Basten, Mesman
	30 min	(107) An Approach to Execute Conditional Branches onto SIMD Multi-Context Reconfigurable Architectures F.Alexander R.Velez, M.S.Martin, M.F. Centeno, N.Bagherzadeh
	30 min	(106) Optimization of a Bus-based Test Data Transportation Mechanism in System-on-Chip *Anders Larsson, Erik Larsson, Petru Eles, Zebo Peng*

10:30-11:00	30 min	Poster Session: Papers [68, 71, 113, 72]
10:30-11:00	30 min	Coffee break
11:00-12:00	60 min	Keynote Speech **Modelling software systems using UML 2.0** *Francois Terrier*
12:00-13:00	60 min	Keynote Speech *Chair K.Kuchcinski* **Networks on Chip** *Hannu Tenhunen*
13:00-14:30	90 min	Lunch

Friday, September 2

14:30-16:30

SS3: Remonte Educational Tools for Design and Testing (S16)
Part 1. ***Chair R. Ubar***

14:30-16:30	30 min	(78) An Educational Environment for Digital Testing: Hardware, Tools, and Web-Based Runtime Platform *Jaan Raik, Raimund Ubar*
	30 min	(119) Educational Tool for the Demonstration of DfT Principles Based on Scan Methodologies *Josef Strnadel, Zdenek Kotasek*
	15 min	(102) REMOTE PATH DELAY FAULT SIMULATION *Øystein Gjermundnes, Einar J. Aas*
	15 min	(84) INTERNET-BASED IC TECHNOLOGY DESIGN AND SIMULATION Nelayev V., Stempitsky V., Kudin K.

Circuits Synthesis (S17)
Part 3. Advanced Logic Synthesis. ***Chair***

14:30-16:30	30 min	(92) Decomposition of Multi-Output Functions for CPLDs *Dariusz Kania, Jozef Kulisz*
	30 min	(124) High-quality Sub-function Construction in the Information-driven Circuit Synthesis with Gates *Lech Jóźwiak, Szymon Biegański*
	30 min	(58) Efficient Implementation of Digital Filters with Use of Advanced Synthesis Methods Targeted FPGA Architectures *M. Rawski, P. Tomaszewicz, H. Selvaraj, T. Łuba*
	30 min	(21) On LUT Cascade Realizations of FIR Filters *Tsutomu Sasao, Yukihiro Iguchi, Takahiro Suzuki*

Performance Optimization: Architecture and Tools (S18)
Part 1. ***Chair K.Kuchcinski***

14:30-16:00	30 min	(108) Run-time Adaptive Resource Allocation and Balancing on Nanoprocessors Arrays *Danilo Pani, Giuseppe Passino, Luigi Raffo*
	30 min	(94) ARPA - A Technology Independent and Synthetizable System-on-Chip Model for Real-Time Applications *A. S. R. Oliveira, V. A. Sklyarov, A. B. Ferrari*
	30 min	(110) Dynamic Split: Flexible Border Between Instruction and Data Cache *Pedro Trancoso*

16:30-17:00	30 min	Coffee break